

# GC864-QUAD V2 Hardware User Guide

1w0300874 Rev.2 – 2010-09-02













## 1.4. Document Organization

This document contains the following chapters:

[Chapter 1: "Introduction"](#) provides a scope for this document, target audience, contact and support information, and text conventions.

[Chapter 2: "Overview"](#) provides an overview of the document.

[Chapter 3: "GC864-QUAD V2 Mechanical Dimensions"](#)

[Chapter 4: "Hardware Commands"](#) How to control the module via hardware.

[Chapter 5: "Power supply"](#) Power supply requirements and general design rules.

[Chapter 6: "Antenna"](#) The antenna connection and board layout design are the most important parts in the full product design

[Chapter 7: "Logic Level specifications"](#) Specific values adopted in the implementation of logic levels for this module.

[Chapter 8: "Serial ports"](#) The serial port on the Telit GC864 is the core of the interface between the module and OEM hardware

[Chapter 9: "Audio Section overview"](#) Refers to the audio blocks of the Base Band Chip of the GC864 Telit Modules.

[Chapter 10: "General Purpose I/O"](#) How the general purpose I/O pads can be configured.

[Chapter 11: "Mounting the GC864-QUAD V2 on the application board"](#) Recommendations and specifics on how to mount the module on the user's board.





## 1.7. Document History

Revision	Date	Changes
ISSUE#0	2010-01-25	Release First ISSUE# 0
ISSUE#1	2010-03-29	Updated Par.4.1, Par.5.1, Par.6.1
ISSUE#2	2010-09-02	Removed GC8764-DUAL V2 §6 updated current consumption table



## 2. Overview

In this document all the basic functions of a mobile phone are taken into account; for each one of them a proper hardware solution is suggested and eventually the wrong solutions and common errors to be avoided are evidenced. Obviously this document cannot embrace the whole hardware solutions and products that may be designed. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configurations shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for properly developing your product with the Telit GC864-QUAD V2 module. For further hardware details that may not be explained in this document refer to the Telit GC864-QUAD V2 Product Description document where all the hardware information is reported.



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### NOTICE:

(EN) The integration of the GSM/GPRS GC864-QUAD V2 cellular module within user application shall be done according to the design rules described in this manual.

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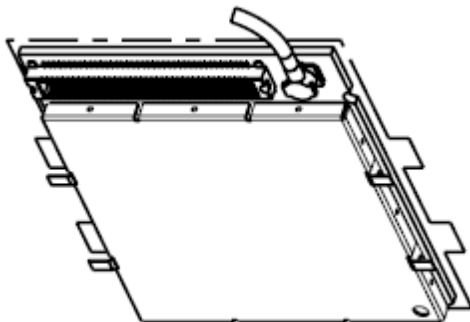
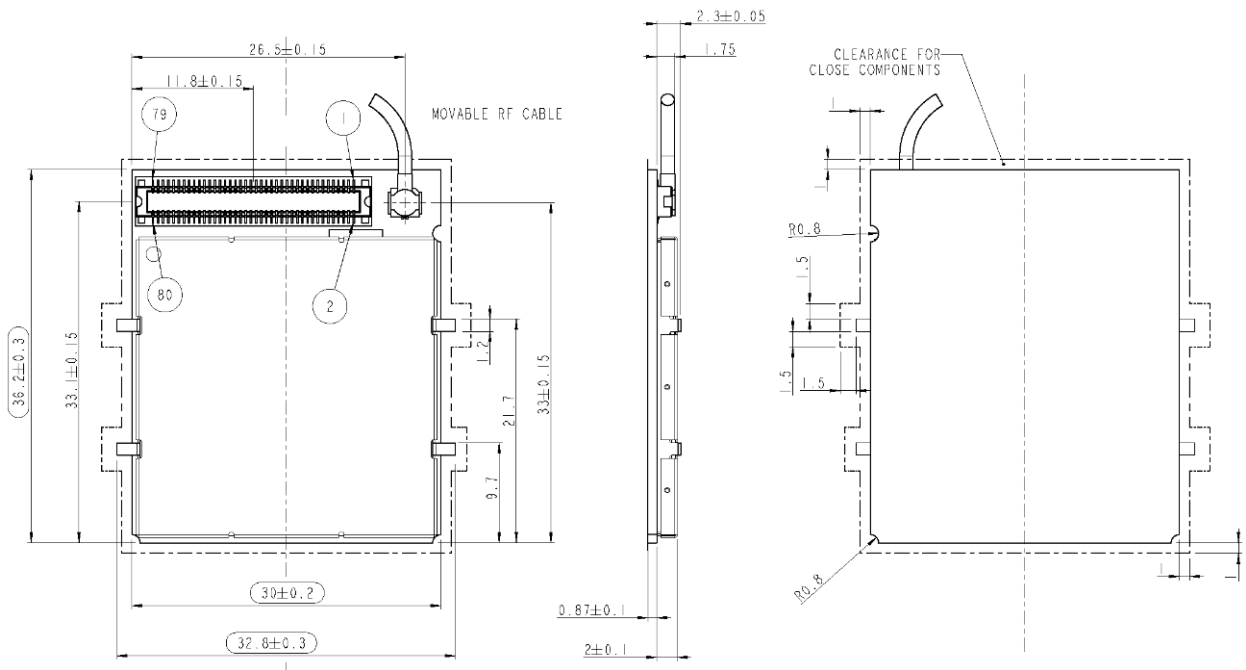
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### 3. GC864 Mechanical Dimensions

The Telit GC864-QUAD V2 module overall dimensions are:

- Length: 36.2 mm
- Width: 30 mm
- Thickness: 3.2 mm
- Weight: 4.8g







## GC864-QUAD V2 Hardware User Guide

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Pin	Signal	I/O	Function	Internal Pull up	Type
<b>Prog. / Data + Hw Flow Control</b>					
25	C103/TXD	I	Serial data input (TXD) from DTE		CMOS 2.8V
26	C104/RXD	O	Serial data output (RXD) to DTE		CMOS 2.8V
27	C107/DSR	O	Output for Data set ready signal (DSR) to DTE		CMOS 2.8V
28	C106/CTS	O	Output for Clear to send signal (CTS) to DTE		CMOS 2.8V
29	C108/DTR	I	Input for Data terminal ready signal (DTR) from DTE		CMOS 2.8V
30	C125/RING	O	Output for Ring indicator signal (RI) to DTE		CMOS 2.8V
31	C105/RTS	I	Input for Request to send signal (RTS) from DTE		CMOS 2.8V
32	C109/DCD	O	Output for Data carrier detect signal (DCD) to DTE		CMOS 2.8V
<b>DAC and ADC</b>					
37	ADC_IN1	AI	Analog/Digital converter input		A/D
38	ADC_IN2	AI	Analog/Digital converter input		A/D
39	ADC_IN3	AI	Analog/Digital converter input		A/D
40	DAC_OUT	AO	Digital/Analog converter output		D/A
<b>Miscellaneous Functions</b>					
45	STAT_LED	O	Status indicator led		CMOS 1.8V
46	GND	-	Ground		Ground
49	PWRMON	O	Power ON Monitor		CMOS 2.8V
53	ON/OFF*	I	Input command for switching power ON or OFF (toggle command). The pulse to be sent to the GC864-QUAD V2 must be equal or greater than 1 second.	47K $\Omega$	Pull up to VBATT
54	RESET*	I	Reset input		
55	VRTC	AO	VRTC Backup capacitor		Power
<b>Telit GPIO / DVI</b>					
36	DVI_CLK	-	DVI_CLK (Digital Voice Interface Clock)		CMOS 2.8V
59	TGPIO_04/TXCNTRL	I/O	Telit GPIO4 Configurable GPIO / RF Transmission Control		CMOS 2.8V
63	TGPIO_10/DVI_TX	I/O	Telit GPIO10 Configurable GPIO / DVI_TX (Digital Voice Interface)		CMOS 2.8V
65	DVI_RX	I/O	DVI_RX (Digital Voice Interface)		CMOS 2.8V
66	TGPIO_03	I/O	Telit GPIO3 Configurable GPIO		CMOS 2.8V
67	TGPIO_08	I/O	Telit GPIO8 Configurable GPIO		CMOS 2.8V
68	TGPIO_06 / ALARM	I/O	Telit GPIO6 Configurable GPIO / ALARM		CMOS 2.8V
70	TGPIO_01	I/O	Telit GPIO1 Configurable GPIO		CMOS 2.8V
71	DVI_WAO	I/O	DVI_WAO (Digital Voice Interface)		CMOS 2.8V
73	TGPIO_07 / BUZZER	I/O	Telit GPIO7 Configurable GPIO / Buzzer		CMOS 2.8V
74	TGPIO_02 / JDR	I/O	Telit GPIO02 I/O pin / Jammer detect report		CMOS 2.8V
76	TGPIO_09	I/O	Telit GPIO9 Configurable GPIO		CMOS 2.8V
78	TGPIO_05/ RFTXMON	I/O	Telit GPIO05 Configurable GPIO / Transmitter ON monitor		CMOS 2.8V
<b>RESERVED</b>					
17	Reserved	-			
33	Reserved	-			



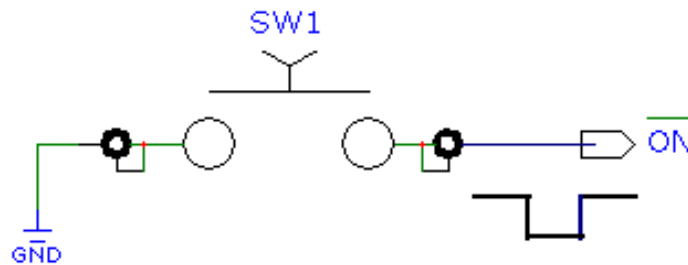




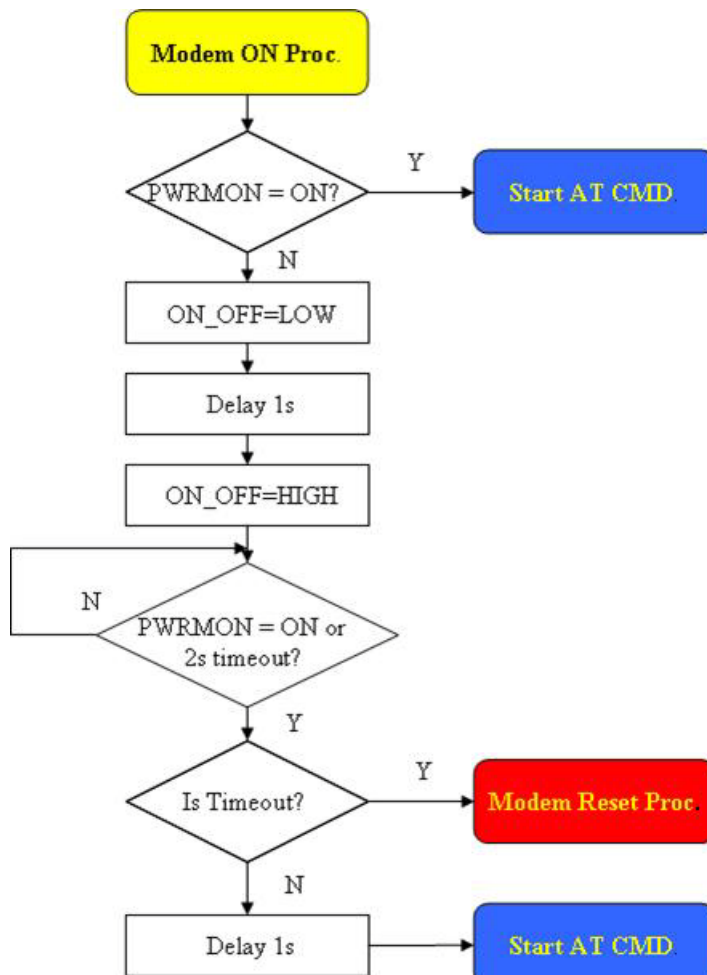


For example:

- 1- Let us assume you need to drive the ON# pad with a totem pole output of a +3/5 V microcontroller (uP\_OUT1):
- 2- Let us assume you need to drive the ON# pad directly with an ON/OFF button:



A flow chart with proper turn on procedure is detailed below:



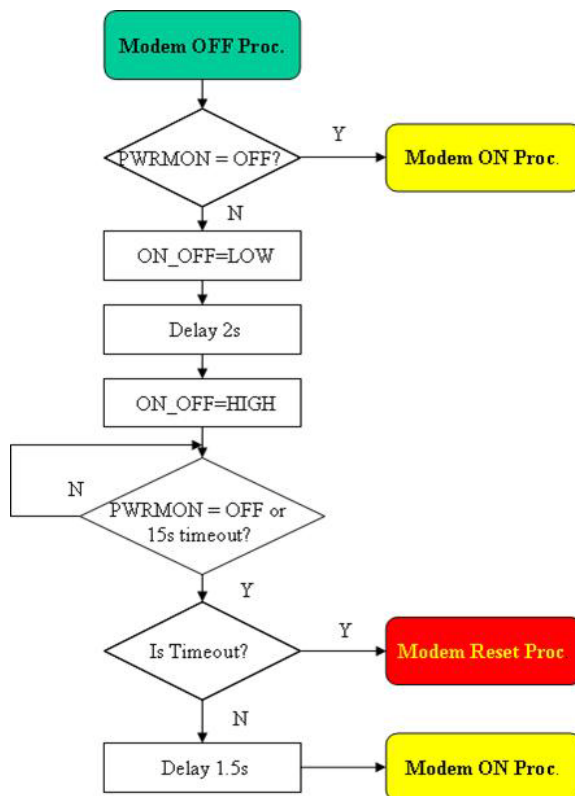
## 4.2. Turning OFF the GC864-QUAD V2

Turning off of the device can be done in three ways:

- by software command (see GC864-QUAD V2 Software User Guide)
- by tying low pin ON#

Either ways, the device issues a detach request to network informing that the device will not be reachable any more. To turn OFF the GC864 via pin ON#, this must be tied low for at least 1000ms and then released. The same circuitry and timing for the power on shall be used. The device shuts down after the release of the ON# pin.

The following flow chart shows the proper turnoff procedure:



### TIP:

To check if the device has powered off, the hardware line PWRMON must be monitored. When PWRMON goes low, then the device has powered off.



### 4.2.1. Hardware Unconditional Restart



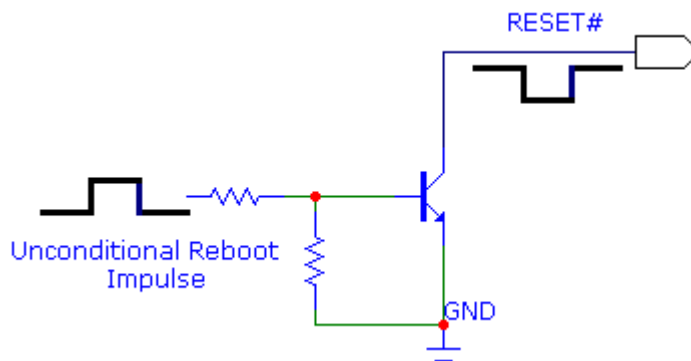
**WARNING:**

The hardware unconditional Restart must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure to be done in the rare case that the device gets stacked waiting for some network or SIM responses.

To unconditionally Restart the GC864-QUAD V2, the pad RESET# must be tied low for at least 200 ms and then released.

The maximum current that can be drained from the RESET# pad is 0,15 mA.

A simple circuit to do it is:



**NOTE:**

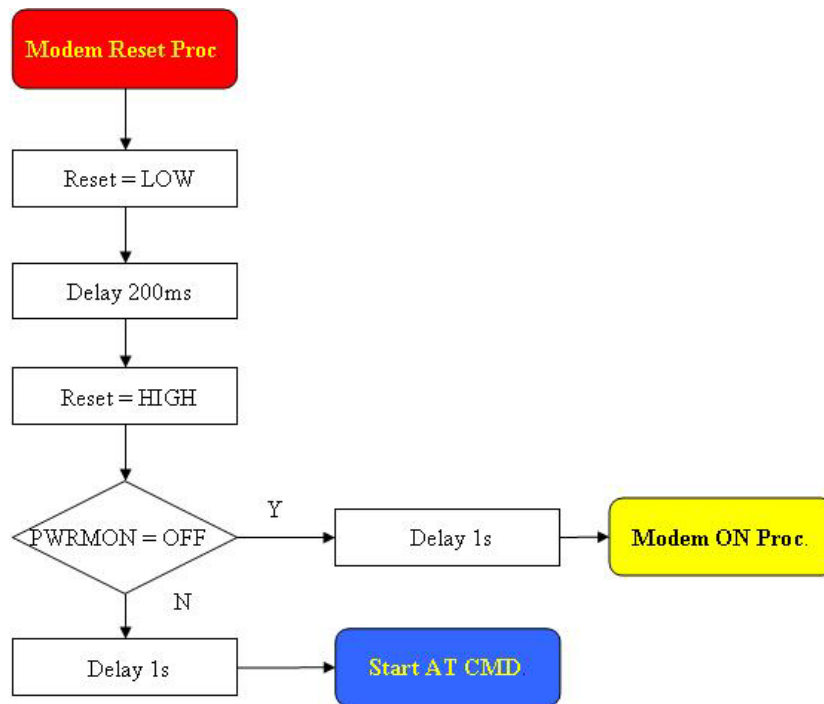
Do not use any pull up resistor on the RESET\* line nor any totem pole digital output. Using pull up resistor may cause latch up problems on the GC864-QUAD V2 power regulator and improper functioning of the module. The line RESET\* must be connected only in open collector configuration.

**TIP:**

The unconditional hardware reboot must always be implemented on the boards and the software must use it as an emergency exit procedure.

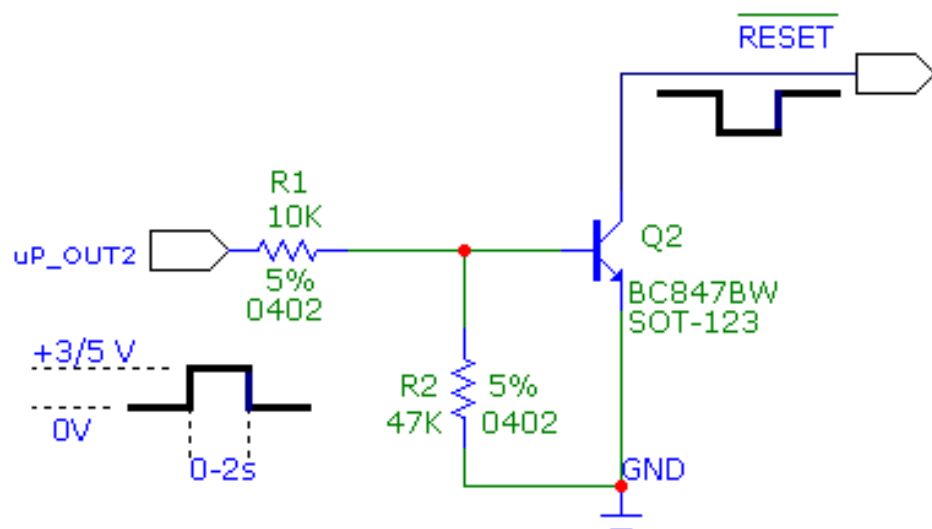


In the following flow chart is detailed the proper restart procedure:



For example:

- 1- Let us assume you need to drive the RESET# pad with a totem pole output of a +3/5 V microcontroller (uP\_OUT2):



## 5. Power Supply

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performances, hence read carefully the following requirements and guidelines for a proper design.

### 5.1. Power Supply Requirements

Condition	Value
Nominal Supply Voltage	3.80 V
Normal operating Voltage Range	3.40 V - 4.20 V
Extended operating Voltage Range	3.22 V - 4.50 V

The GC864-QUAD V2 power consumptions are:

GE864-QUAD V2		
Mode	Average (mA)	Mode description
<b>SWITCHED OFF</b>		
Switched Off	<62 uA	Module supplied but Switched Off
<b>IDLE mode</b>		
AT+CFUN=1	16.0	Normal mode: full functionality of the module
AT+CFUN=4	16.0	Disabled TX and RX; module is not registered on the network
AT+CFUN=0 or =5	3.9	Paging Multiframe 2
	2.5	Paging Multiframe 3
	2.4	Paging Multiframe 4
	1.5	Paging Multiframe 9
<b>CSD TX and RX mode</b>		
GSM900 CSD PL5	240	GSM VOICE CALL
DCS1800 CSD PL0	175	
<b>GPRS (class 10) 1TX</b>		
GSM900 PL5	225	GPRS Sending data mode
DCS1800 PL0	160	
<b>GPRS (class 10) 2TX</b>		
GSM900 PL5	420	GPRS Sending data mode
DCS1800 PL0	290	



The GSM system is made in a way that the RF transmission is not continuous but it is packed into bursts at a base frequency of about 216 Hz. The relative current peaks can be as high as about 2A. Therefore the power supply has to be designed in order to withstand with these current peaks without big voltage drops; this means that both the electrical design and the board layout must be designed for this current flow.

If the layout of the PCB is not well designed, then a strong noise floor is generated on the ground and the supply; this will reflect on all the audio paths producing an audible and annoying noise at 216 Hz; if the voltage drop during the peak current absorption is too much, then the device may even shutdown as a consequence of the supply voltage drop.



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**TIP:**

The power supply must be designed so that it is capable of a peak current output of at least 2 A.

**TIP:**

the supply voltage is directly measured between VBATT and GND pins. It must stay within the Wide Supply Voltage tolerant range including any drop voltage and overshoot voltage (during the slot tx, for example).

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**NOTE:** The Operating Voltage Range **MUST** never be exceeded also in power off condition; care must be taken in order to fulfill min/max voltage requirement

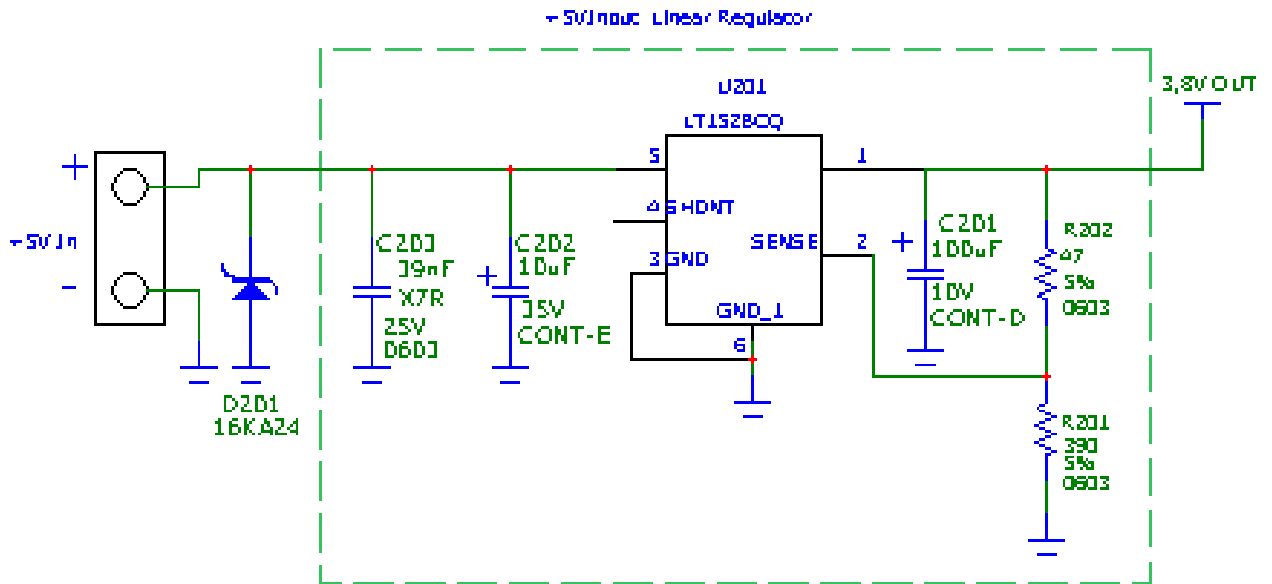
**NOTE:** When the power supply voltage is lower than 3.4V, to turn ON the module, the pad ON# must be tied low for at least 3 seconds.

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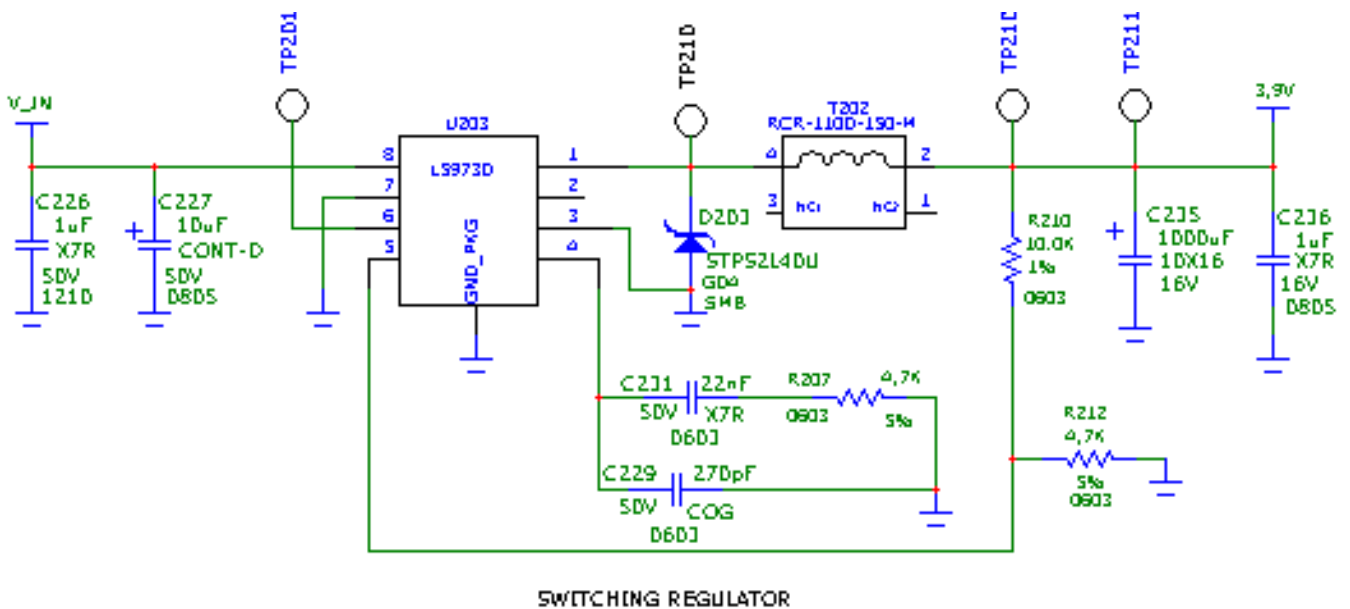
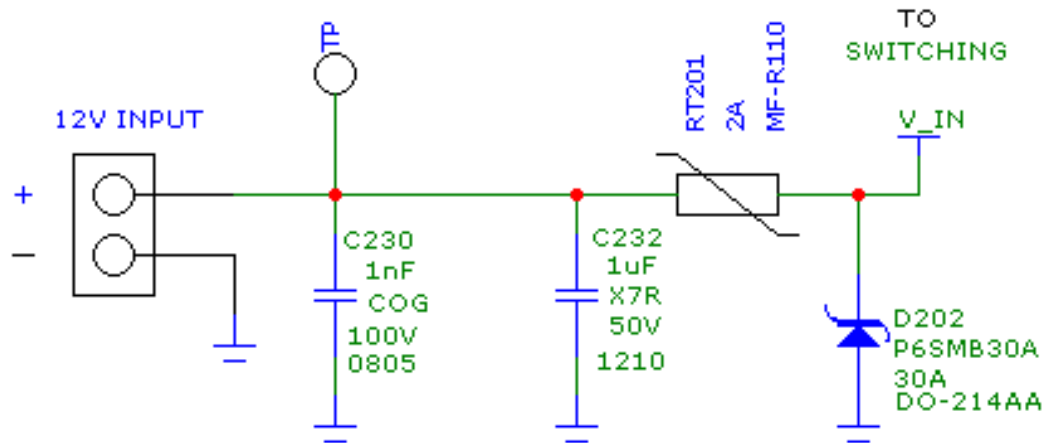


An example of linear regulator with 5V input is:





An example of switching regulator with 12V input is in the schematic below (split in 2 parts):







- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when the 2A current peaks are absorbed. Note that this is not made in order to save power loss but especially to avoid the voltage drops on the power line at the current peaks frequency of 216 Hz that will reflect on all the components connected to that supply, introducing the noise floor at the burst base frequency. For this reason while a voltage drop of 300-400 mV may be acceptable from the power loss point of view, the same voltage drop may not be acceptable from the noise point of view. If your application does not have audio interface but only uses the data feature of the Telit GC864-QUAD V2, then this noise is not so disturbing and power supply layout design can be more forgiving.
- The PCB traces to the GC864-QUAD V2 and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur when the 2A current peaks are absorbed. This is for the same reason as previous point. Try to keep this trace as short as possible.
- The PCB traces connecting the Switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for switching power supply). This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).
- The use of a good common ground plane is suggested.
- The placement of the power supply on the board must be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables must be kept separate from noise sensitive lines such as microphone/earphone cables.

#### 5.2.4. Parameters for ATEX Applications

In order to integrate the Telit GC864-QUAD V2 module into an ATEX application, the appropriate reference standard IEC EN xx and integrations shall be followed.

Below are listed parameters and useful information to integrate the module in your application:

- Total capacity: 27.45 uF
- Total inductance: 55.20 nH
- No voltage upper than supply voltage is present in the module.









## 7. Logic Level Specifications

Where not specifically stated, all the interface circuits work at 2.8V CMOS logic levels. The following table shows the logic level specifications used in the Telit GC864-QUAD V2 interface circuits:

### Absolute Maximum Ratings – Not Functional

Parameter	Min	Max
Input level on any digital pin when on	-0.3V	+3.1V
Input voltage on analog pins when on	-0.3V	+3.0 V

### Operating Range – Interface Levels (2.8V CMOS)

Level	Min	Max
Input high level	2.1V	3.1V
Input low level	0V	0.5V
Output high level	2.2V	3.0V
Output low level	0V	0.35V

For 1,8V signals:

### Operating Range – Interface Levels (1.8V CMOS)

Level	Min	Max
Input high level	1.6V	2.2V
Input low level	0V	0.4V
Output high level	1,65V	2.2V
Output low level	0V	0.35V

### Current characteristics

Level	Typical
Output Current	1mA
Input Current	1uA







**Operating Range – Interface Levels (2.8V CMOS)**

Level	Min	Max
Input high level $V_{IH}$	2.1V	3.1V
Input low level $V_{IL}$	0V	0.5V
Output high level $V_{OH}$	2.2V	3.0V
Output low level $V_{OL}$	0V	0.35V

The table below shows the signals of the GC864-QUAD V2 serial port:

RS232 Pin Number	Signal	GC864-QUAD V2 Pad Number	Name	Usage
1	DCD – dcd_uart	32	Data Carrier Detect	Output from the GC864-QUAD V2 that indicates the carrier presence
2	RXD – tx_uart	26	Transmit line *see Note	Output transmit line of GC864-QUAD V2 UART
3	TXD – rx_uart	25	Receive line *see Note	Input receive of the GC864-QUAD V2 UART
4	DTR – dtr_uart	29	Data Terminal Ready	Input to the GC864-QUAD V2 that controls the DTE READY condition
5	GND	5,6,7	Ground	ground
6	DSR – dsr_uart	27	Data Set Ready	Output from the GC864-QUAD V2 that indicates the module is ready
7	RTS – rts_uart	31	Request to Send	Input to the GC864-QUAD V2 that controls the Hardware flow control
8	CTS – cts_uart	28	Clear to Send	Output from the GC864-QUAD V2 that controls the Hardware flow control
9	RI – ri_uart	30	Ring Indicator	Output from the GC864-QUAD V2 that indicates the incoming call condition



**\*NOTE:**

According to V.24, RX/TX signal names are referred to the application side, therefore on the GC864-QUAD V2 side these signal are on the opposite direction: TXD on the application side will be connected to the receive line (here named TXD/ rx\_uart ) of the GC864-QUAD V2 serial port and vice versa for RX.

**TIP:**

For a minimum implementation, only the TXD and RXD lines can be connected, the other lines can be left open provided a software flow control is implemented.

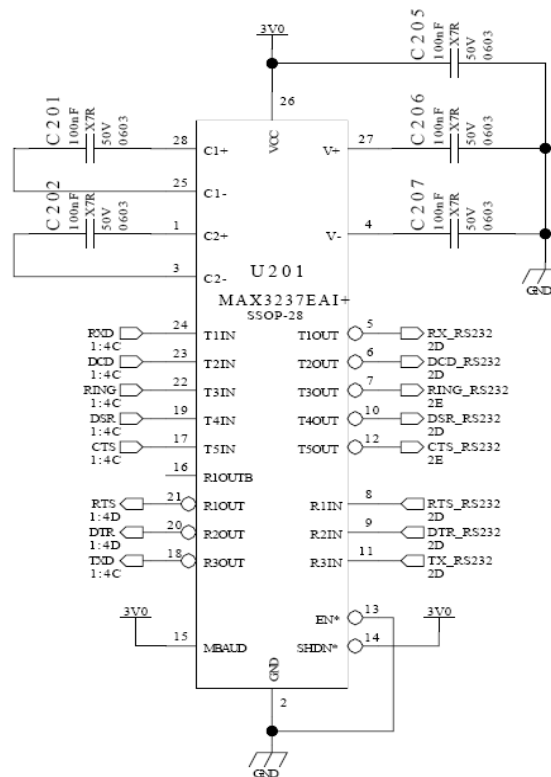




**NOTE:**

In order to be able to do in circuit reprogramming of the GC864-QUAD V2 firmware, the serial port on the Telit GC864-QUAD V2 shall be available for translation into RS232 and either it is controlling device shall be placed into tristate, disconnected or as a gateway for the serial data when module reprogramming occurs. Only RXD, TXD, GND, SERVICE and the On/off module turn on pad are required to the reprogramming of the module, the other lines are unused. All applicator shall include in their design such a way of reprogramming the GC864-QUAD V2.

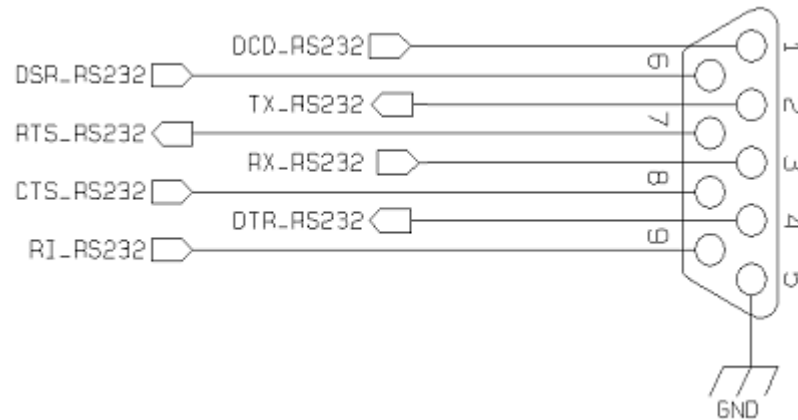
An example of level translation circuitry of this kind is:



RS232 LEVEL TRSANSULATOR

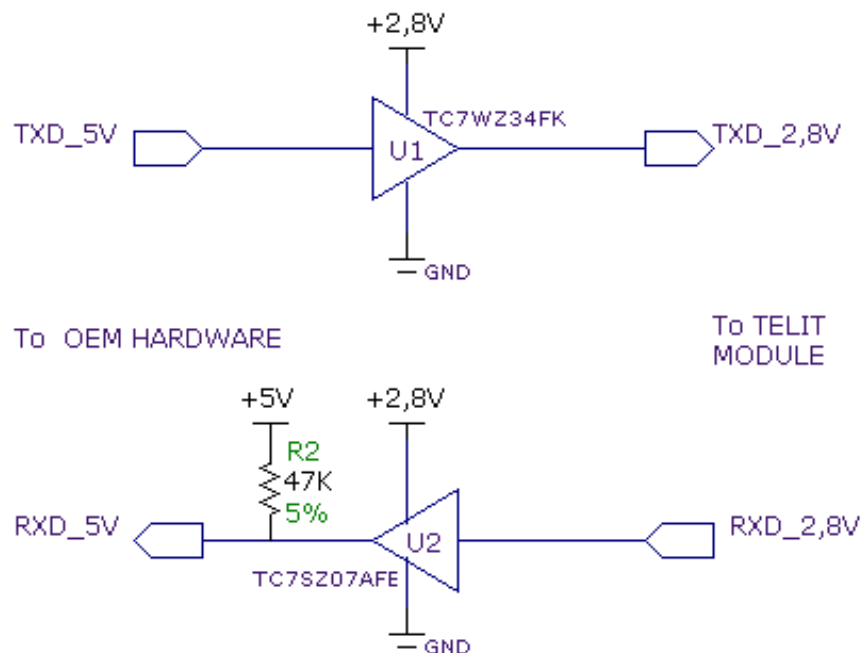


The RS232 serial port lines are usually connected to a DB9 connector with the following layout:



### 8.3. 5V UART Level Translation

If the OEM application uses a microcontroller with a serial port (UART) that works at a voltage different from 2.8 – 3V, then a circuitry has to be provided to adapt the different levels of the two set of signals. As for the RS232 translation there are a multitude of single chip translators. For example a possible translator circuit for a 5V TRANSMITTER/RECEIVER can be:





## 9. Audio Section Overview

The first Baseband chip was developed for the cellular phones, which needed two separated amplifiers both in RX and in TX section.

A couple of amplifiers had to be used with internal audio transducers while the other couple of amplifiers had to be used with external audio transducers.

To distinguish the schematic signals and the Software identifiers, two different definitions were introduced, with the following meaning:

- internal audio transducers → *HS/MT* (from *HandSet* or *MicroTelephone* )
- external audio transducers → *HF* (from *HandsFree* )

Actually the acronyms have not the original importance.

In other words this distinction is not necessary, being the performances between the two blocks like the same.

Only if the customer needs higher output power to drive the speaker, he needs to adopt the Aduio2 Section ( *HF* ). Otherwise the choice could be done in order to overcome the PCB design difficulties.

For these reasons we have not changed the *HS* and *HF* acronyms, keeping them in the Software and on the schematics.

The Base Band Chip of the GC864-QUAD V2 Telit Modules maintains the same architecture.

For more information and suggestions refer to Telit document:

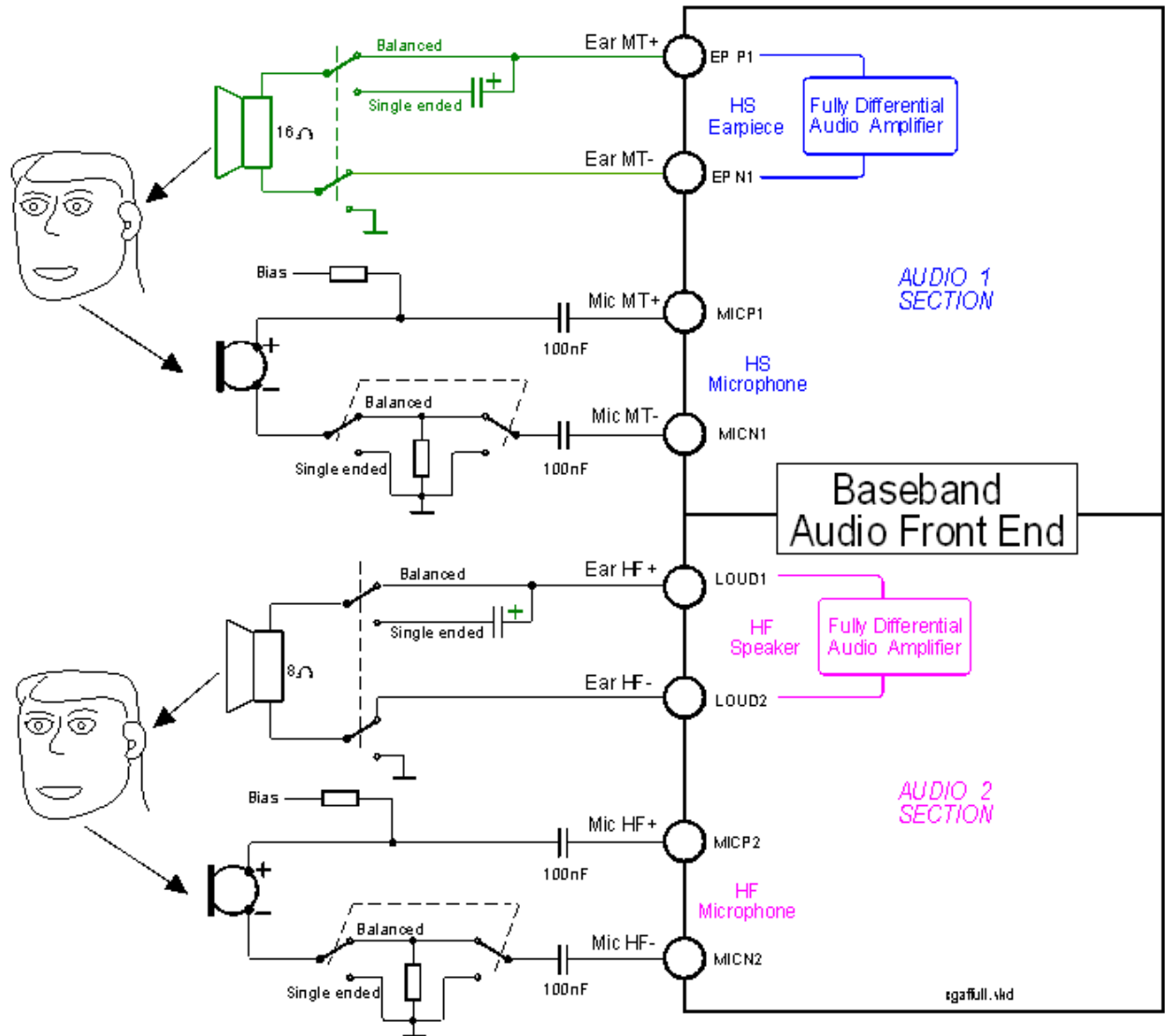
- Audio settings application note , 80000NT10007a

### 9.1. Selection mode

Only one block can be active at a time, and the activation of the requested audio path is done via hardware ,by *AXE* line, or via software ,by *AT#CAP* command .

Moreover the *Sidetone* functionality could be implemented by the amplifier fitted between the transmit path and the receive path, enabled at request in both modes.





GC864-QUAD V2 Audio Front End Block Diagram



## 9.2. Electrical Characteristics



**TIP:** Being the microphone circuitry the more noise sensitive, its design and layout must be done with particular care. Both microphone paths are balanced and the OEM circuitry must be balanced designed to reduce the common mode noise typically generated on the ground plane. However the customer can use the unbalanced circuitry for its particular application.

### 9.2.1. Input Lines Characteristics

"MIC_MT" and "MIC_HF" differential microphone paths	
Line Coupling	AC*
Line Type	Balanced
Differential input voltage	$\leq 1,03V_{pp}$ @ <i>Mic G=0dB</i>
Gain steps	7
Gain increment	6dB per step
Coupling capacitor	$\geq 100nF$
Differential input resistance	50K $\Omega$
Input capacitance	$\leq 10pF$



**(\*) WARNING :** AC means that the signals from the microphone have to be connected to input lines of the module through capacitors which value has to be  $\geq 100nF$ . Not respecting this constraint, the input stages will be damaged.

**WARNING:** when particular OEM application needs a *Single Ended Input* configuration, it is forbidden connecting the unused input directly to Ground, but only through a 100nF capacitor. Don't forget that the useful input signal will be halved in *Single Ended Input* configuration.







## 10. General Purpose I/O

The general-purpose I/O pads can be configured to act in three different ways:

- Input
- Output
- Alternate function (internally controlled)

Input pads can only be read and report the digital value (high or low) present on the pad at the read time; output pads can only be written or queried and set the value of the pad output; an alternate function pad is internally controlled by the GC864-QUAD V2 firmware and acts depending on the function implemented.

The following GPIO are available on the GC864-QUAD V2:

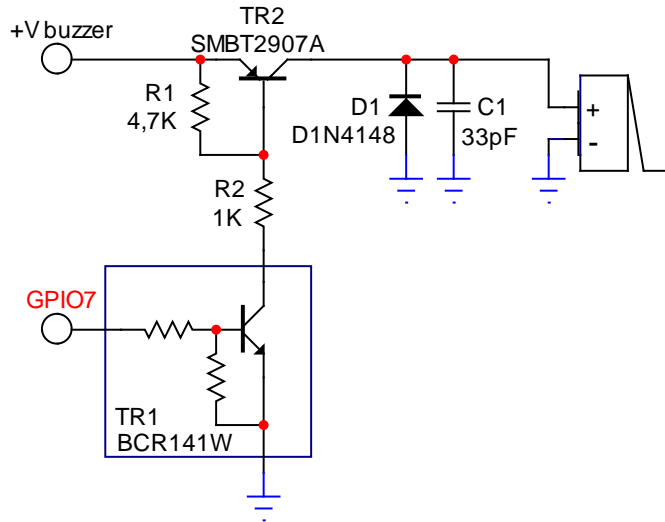
Pin	Signal	I/O	Function	Type	Input / output current	Default state	ON_OFF state	During Reset state	Note
70	TGPIO_01	I/O	GPIO01 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0	0	
74	TGPIO_02 / JDR	I/O	GPIO02 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0	0	Alternate function (JDR)
66	TGPIO_03	I/O	GPIO03 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0	0	
59	TGPIO_04 / TXCNTRL	I/O	GPIO04 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0	0	Alternate function (RF Transmission Control)
78	TGPIO_05 / RFTXMON	I/O	GPIO05 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0	0	Alternate function (RFTXMON)
68	TGPIO_06 / ALARM	I/O	GPIO06 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0	0	Alternate function (ALARM)
73	TGPIO_07 / BUZZER	I/O	GPIO07 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0	0	Alternate function (BUZZER)
67	TGPIO_08	I/O	GPIO08 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0	0	
76	TGPIO_09	I/O	GPIO09 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0	0	
63	TGPIO_10 / DVI_TX	I/O	GPIO10 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0	0	Alternate function (DVI_TX)











Example of Buzzer's driving circuit



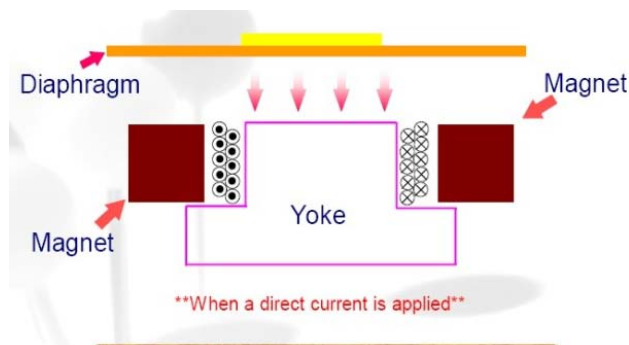
**NOTE:**

To correctly drive a buzzer, a driver must be provided; its characteristics depend on the Buzzer and for them refer to your buzzer vendor.

## 10.8. Magnetic Buzzer Concepts

### 10.8.1. Short Description

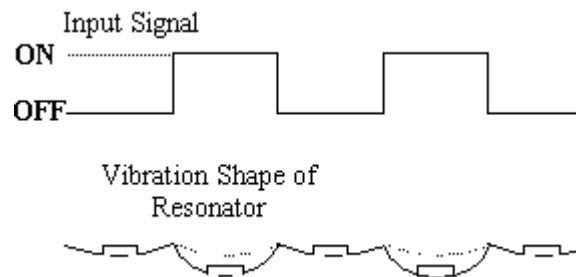
A magnetic Buzzer is a sound-generating device with a coil located in the magnetic circuit consisting of a permanent magnet, an iron core, a high permeable metal disk, and a vibrating diaphragm.



Drawing of the Magnetic Buzzer



The disk and diaphragm are attracted to the core by the magnetic field. When an oscillating signal is moved through the coil, it produces a fluctuating magnetic field, which vibrates the diaphragm at a frequency of the drive signal. Thus the sound is produced relative to the frequency applied.



*Diaphragm movement*

### 10.8.2. Frequency Behavior

The frequency behavior represents the effectiveness of the reproduction of the applied signals.

Because its performance is related to a square driving waveform (whose amplitude varies from 0V to Vpp), if you modify the waveform (e.g. from square to sinus) the frequency response will change.

### 10.8.3. Power Supply Influence

Applying a signal whose amplitude is different from that suggested by manufacturer, the performance change following the rule:

if resonance frequency  $f_0$  increases, amplitude decreases.

Because of resonance frequency depends from acoustic design, lowering the amplitude of the driving signal the response bandwidth tends to become narrow, and vice versa.

Summarizing:  $V_{pp} \uparrow \rightarrow f_0 \downarrow$                        $V_{pp} \downarrow \rightarrow f_0 \uparrow$

The risk is that the  $f_0$  could easily fall outside of new bandwidth; consequently the SPL could be much lower than the expected.

### 10.8.4. Warning

It is very important to respect the sense of the applied voltage: never apply to the “-“ pin a voltage more positive than the “+“ pin. If this happens, the diaphragm vibrates in the opposite sense with a high probability to be expelled from its physical position, damaging the device forever.





## 10.10. Indication of Network Service Availability

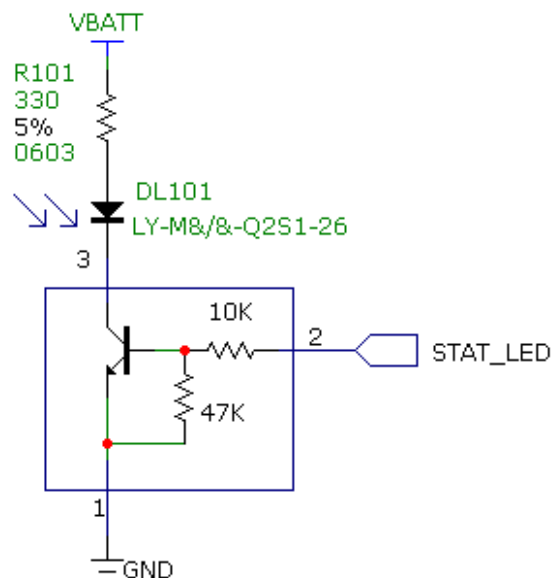
The STAT\_LED pin status shows information on the network service availability and Call status.

In the GC864-QUAD V2 modules, the STAT\_LED usually needs an external transistor to drive an external LED.

Therefore, the status indicated in the following table is reversed with respect to the pin status.

LED status	Device Status
Permanently off	Device off
Fast blinking (Period 1s, Ton 0,5s)	Net search / Not registered / turning off
Slow blinking (Period 3s, Ton 0,3s)	Registered full service
Permanently on	a call is active

A schematic example could be:



## 10.11. RTC Bypass Out

The VRTC pin brings out the Real Time Clock supply, which is separate from the rest of the digital part, allowing having only RTC going on when all the other parts of the device are off.

To this power output a backup capacitor can be added in order to increase the RTC autonomy during power off of the battery. NO Devices must be powered from this pin.

## 10.12. DAC Converter

### 10.12.1. Description

Pin	Signal	I/O	Function	Internal Pull up	Type
<b>DAC Converter</b>					
40	DAC_OUT	AO	Digital/Analog converter output		D/A

The GC864-QUAD V2 module provides one Digital to Analog Converter.

The on board DAC is a 10-bit converter, able to generate a analogue value based a specific input in the range from 0 up to 1023. However, an external low-pass filter is necessary.

	Min	Max	Units
Voltage range (filtered)	0	2,6	Volt
Range	0	1023	Steps

The precision is 10 bits, so if we consider that the maximum voltage is 2V, the integrated voltage could be calculated with the following formula:

$$\text{Integrated output voltage} = 2 * \text{value} / 1023$$

DAC\_OUT line must be integrated (for example with a low band pass filter) in order to obtain an analog voltage.

### 10.12.2. Enabling DAC

The AT command below is available to use the DAC function:

**AT#DAC[=<enable>[,<value>]]**

<value> – scale factor of the integrated output voltage (0–1023, with 10 bit precision), and it must be present if <enable>=1.





The on board A/D are 11-bit converter. They are able to read a voltage level in the range of 0÷2 volts applied on the ADC pin input, store and convert it into 11 bit word.

	Min	Max	Units
Input Voltage range	0	2	Volt
AD conversion	-	11	bits
Resolution	-	< 1	mV

### 10.13.2. Using ADC Converter

The AT command below is available to use the ADC function:

**AT#ADC=1,2**

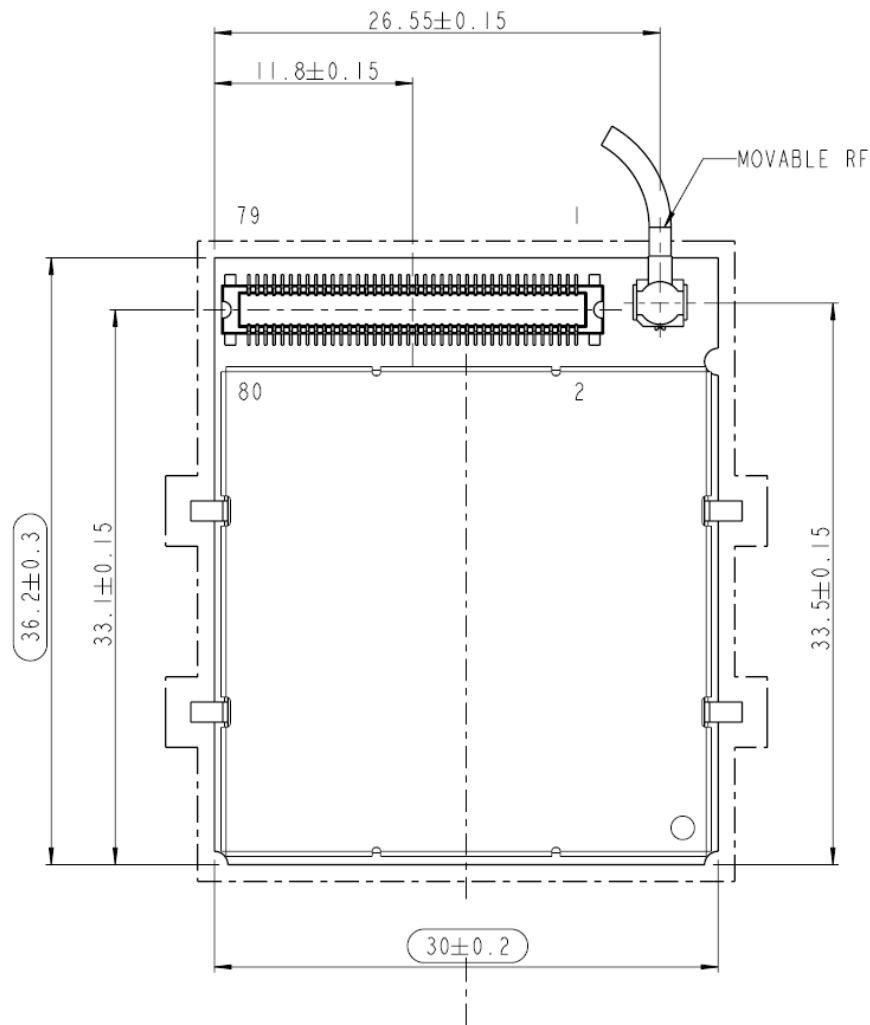
The read value is expressed in mV.

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.



## 11. Assembly the GC864-QUAD V2 on the Board

The position of the Molex board to board connector and the pin 1 are shown in the following picture.



### NOTE:

The metal tabs present on GC864-QUAD V2 must be connected to GND.

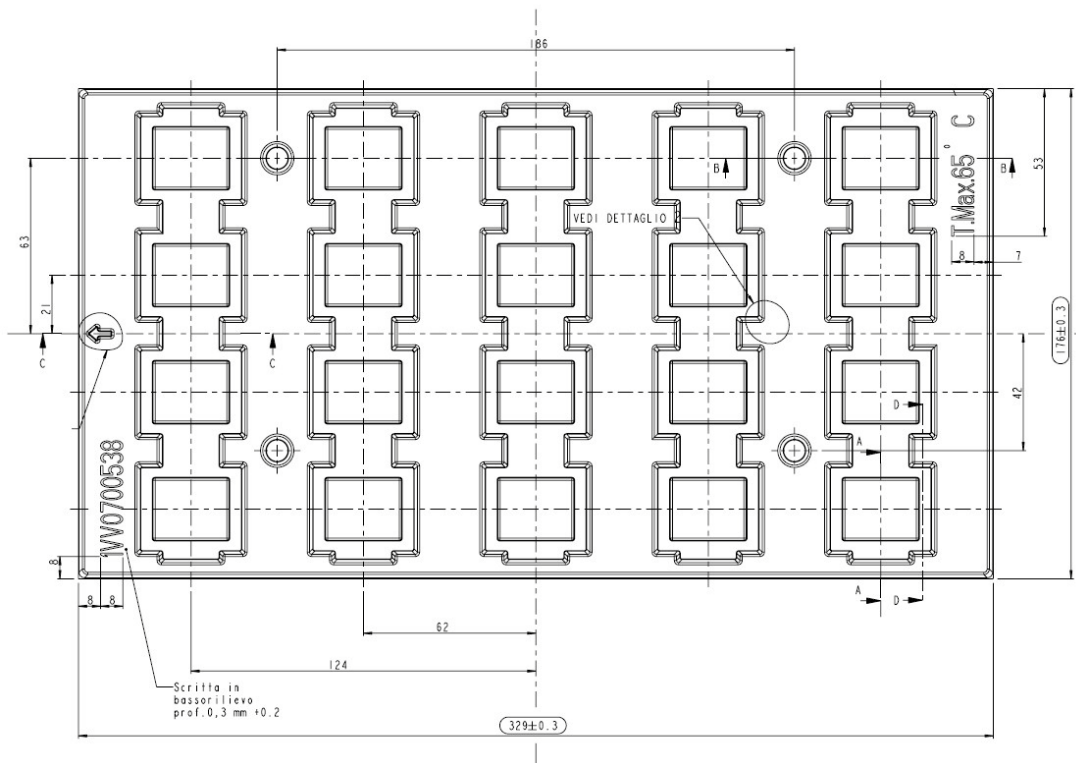
This module could not be processed with a reflow.





## 12. Packing System

The Telit GC864-QUAD V2 are packaged on trays of 20 pieces each.



The size of the tray is: 329 x 176mm.



### WARNING:

These trays can withstand at the maximum temperature of 65° C.







## 14. SAFETY RECOMMENDATIONS



### NOTE:

Read this section carefully to ensure the safe operation.

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc
- Where there is risk of explosion such as gasoline stations, oil refineries, etc

It is responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity.

We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conforming to the security and fire prevention regulations.

The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible of the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as of any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force.

Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case of this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation EN 50360.



